REMARKS

Claims 1-28 were presented for examination and were pending in this application. In an Official Action dated October 19, 2004, claims 1-28 were rejected. Applicants thank Examiner for examination of the claims pending in this application and address Examiner's comments below.

Applicants herein amend claims 1-3, 5, 13, 14, 17, 19, and 20-22. Claims 29-55 are added. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC 102

In the first paragraph of the Office Action, Examiner rejects claims 1-3, 13-17, 19 and 21-24 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,542,991 to Joy et al. ("Joy"). This rejection is now traversed.

Independent claim 1 has been amended to clarify the predetermined nature of the fixed schedule according to which threads are executed. In addition, the "embedded" limitation has been removed to broaden the claim's scope. Independent claim 1, as now amended, recites elements to indicate that the thread scheduling and selection is performed by the processor's hardware thread scheduler, which is

> configurable to allocate available processing time of the processor among at least the first and second threads by causing thread-switching according to a predetermined fixed schedule.

The scheduler is configurable to cause the processor to switch from one thread to another thread within predetermined time periods. This is greatly beneficial because it provides a predictable execution time for threads.

By contrast, Joy simply describes conventional event driven thread scheduling in a multithreaded processor. The conventional multithreading described in Joy is intended for utilizing processor resources efficiently when a thread is stalled. See Joy, col. 6, lines 21-24. That is, the multithreading in Joy is for efficient use of the processor, to reduce "wasted cycle times resulting from stalling and idling." See Joy, col. 2, lines 17-19. The thread switch logic of Joy includes "multithreaded-type functionality in response to an exception condition." (Joy, col. 15, lines 8-11). The context switches in Joy "typically are made in response to interrupts, including hardware and software interrupts, both internal and external, of a processor." Joy, col. 14, lines 62-63. Unlike the thread-switching recited in claim 1, the thread switching in Joy is not due to a predetermined fixed schedule; instead Joy's thread-switching is based on some external stimulus or signal, e.g., L1 data cache miss stall signal, instruction buffer empty signal, etc. (see Joy, col. 3, lines 28-56). Although the priority of execution between threads in Joy may be fixed, the execution of the threads is not according

to a predetermined fixed schedule because the signals or other stimuli that cause the thread switch are external to the scheduler and occur at random times, e.g., a cache miss does not take place according to a predetermined fixed schedule.

Accordingly, for at least this reason, claim 1 is patentable over Joy. Applicants note that new claims 29-45 depend, directly or indirectly, from claim 1. Accordingly, they include the elements described above that are lacking in Joy. Hence, for at least the reasons set forth above, newly added claims 29-45 are also patentable over Joy. Applicants further note that new claim 46 also recites elements that include predetermined fixed schedule thread-switching similar to that recited in claim 1. Hence, for at least the reason described above with respect to claim 1, claim 46 and its dependent claims 47-55 are also patentable over Joy.

Claim 17 is also distinguishable from Joy. Claim 17 recites that the processor "switches from said first thread state to said second thread state between consecutive instruction cycles." This allows the processor to perform "zero-time" context switching, which greatly increases the processor's speed.

Joy describes "fast, nanosecond range context switching." Joy, col. 14, line 48. However, the context switching described in Joy does not take place between consecutive instruction cycles. However fast it may be, the switching described in Joy produces an overhead of at least one processor cycle. See Joy, col. 16, lines 4-5. As described in Joy, "[t]he thread switch logic supports fast thread switch with a very small delay, for example three cycles or less." Joy, col. 16, lines 61-62 (emphasis added). Clearly, the thread switch logic of Joy, requires at least one cycle because it requires response to an external signal (see, col. 16, lines 1-5). In contrast, the processor recited in claim 17 switches between threads in

consecutive cycles; it performs zero-cycle switching. Therefore, for at least this reason, claim 17 and its dependent claims 2-16 and 18, are patentable over Joy.

As shown above, claims 1-3, 13-17, 19 and 21-24 are patentable over the cited reference. Therefore, Applicants kindly request withdrawal of this rejection.

Response to Rejections Under 35 USC 103

In the 14th paragraph of the Office Action, Examiner rejects claims 4 and 20 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of U.S. Patent No. 6,567,839 to Borkenhagen et al. ("Borkenhagen"). Similarly, in the 16th paragraph of the Office Action, Examiner rejects claims 5-9, 18, and 25-28 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of U.S. Patent No. 6,085,215 to Ramakrishnan et al. ("Ramakrishnan"). And in the 23rd paragraph of the Office Action, Examiner rejects claims 10-12 under 35 USC § 103(a) as allegedly being unpatentable over Joy in view of Ramakrishnan and further in view of U.S. Patent No. 6,026,503 to Gutgold et al. ("Gutgold"). This rejections are respectfully traversed.

The rejected claims, 4-9, 10-12, 18, 20, and 25-28, are dependent, directly or indirectly on claims 17 and 19. Both claims 17 and 19 recite the consecutive-cycle context switching elements discussed above, which are lacking in the Joy reference.

The Examiner cited Borkenhagen to make up for the deficiency of a "state selection register" in Joy. However, the combined Joy- Borkenhagen reference still fails to teach or suggest the consecutive-cycle switching recited in the claims. If fact, the system of Borkenhagen incurs the conventional "latency and performance penalties associated with switching threads." (Borkenhagen, col. 15:37-38).

> In the multithreaded processor in the preferred embodiment described herein, this latency includes the time required to complete execution of the current thread to a point where it can be interrupted and correctly restarted when it is next invoked, *the time required to switch the thread-specific hardware facilities from the current thread's state to the new thread's state*, and the time required to restart the new thread and begin its execution.

Borkenhagen, col. 15:38-46 (emphasis added).

Likewise, Ramakrishnan is cited to make up for Joy's lack of "thread identifier for identifying at least one hard-real-time (HRT) thread and at least one non-real-time thread" limitation. However, the Joy-Ramakrishnan combined reference still fails to teach or suggest the consecutive-cycle context switching recited in the claims. Ramakrishnan simply describes a software scheduler that uses a round robin approach to thread scheduling using conventional context switching. See Ramakrishnan, col. 9, lines 9-10. The switching in Ramakrishnan, like in Borkenhagen, is conventional context switching that involves "an associated overhead in invoking the new thread." Ramakrishnan, col. 12, lines 61-62, see also, col. 13, lines 6-7 ("avoid time consuming context switching").

Finally, Gutgold is relied upon to provide the different access speed memory devices recited in claims 10-12 that are not explicitly described in Joy or Ramakrishnan. However, the combined Joy-Ramakrishnan-Gutgold reference still fails to teach or suggest the consecutive-cycle context switching recited in the claims. Gutgold does not describe any context switching. Aside from the fact that Gutgold describes a microprocessor controlled system and associated microprocessor system components, Applicants see no other relation to Applicants' invention.

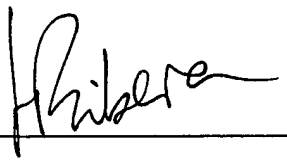
Accordingly, for at least the reasons set forth above, claims 4-9, 10-12, 18, 20, and 25-28 are patentable over the cited combined references. Thus, Applicants kindly request withdrawal of these rejections.

Conclusion

Applicants have added new claims 29-55 for which Applicants request consideration and examination. Applicants respectfully submit that these are supported by the specification and are commensurate within the scope of protection to which Applicants believe they are entitled. Accordingly, Applicants respectfully request allowance of all pending claims.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
NICHOLAS J. KELSEY, ET AL.

Date: Jan 18, 2005 By: 

Hector J. Ribera, Esq.
Registration No. 54,397
FENWICK & WEST LLP
801 California Street
Mountain View, CA 94041
Phone: (650) 335-7192
Fax: (650) 938-5200
E-Mail: hribera@fenwick.com